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Design of a wide band low noise amplifier

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Abstract—The article you are about to read holds the proposition of a wideband low noise amplifier operating in the microwave frequency band starting from 0.5GHz ending at 5GHz, the article includes all steps of LNA design from DC biasing, to wideband matching. It also includes simulation results of each step of the design process. The introduced LNA is a two stage device, the first stage is a pre-amplifier with a low noise figure, the second one is a high gain amplifier, that is to reach a topology with a high gain and low noise figure across the whole operating band simultaneously. The simulation results are then compared to datasheets of LNA devices to decide the performance level of the proposed device.

Index Terms—LNA, pre-amplifier, high gain amplifier, noise figure, stability factor, reflection coefficients, gain compression, OIP3, IIP3.

I. INTRODUCTION

STUDYING telecommunication systems from their early time to recent days, makes the use of low noise amplifiers after the antenna in the reception part of a standard communication link primordial, as it has been developed efficiently with the development of electronic devices [1]. As modern communication systems are based on high frequencies to achieve low design dimensions and high throughput; their transmitted signals experience high attenuation through the transmission channel [2] in addition to path loss [3]. On another hand several types of noise may drown the useful signal beneath their power level. Consequently an amplifier with low internal noise and high power gain have to be designed to extract useful signals from within the noise spectrum without amplifying the noise itself.

The circuit proposed in this article is a two stage topology designed on the theoretical fact that noise factors are divided by the gain of the previous stages, and that the overall gain of the network is equal to the addition of the gain of each stage, if designed well the two stage amplifying network will yield a low noise amplifier with a low noise figure and a high power gain which is desired in communication links.

As second challenge which is that the proposed LNA have to be of a wide operating frequency range, that is to meet the requirements of systems operating from several hundreds of megahertz up to several gigahertz, this relays on designing an LNA that the characteristics are the stated in table:I over the whole operating frequency band.

The devices gain linearity is never to be forgotten as broadband applications signals will suffer from harmonic amplitude distortion because the harmonics constituting the signals are not amplified equally by means of the LNA [4]. This never omits the usability of devices with poor gain flatness as they are used in narrow band applications such as radar systems.

Parameter	Value
Bandwidth	[0.5 – 5]GHz
Gain	$\geq 10dB$
Noise figure	$\leq 3dB$
Stability factor	> 1
S_{11}	$\leq -10dB$

TABLE I: Proposed LNA specifications

II. THEORETICAL CONSIDERATIONS

A. Amplifier gain

Power gain is a crucial parameter in a low noise amplifier, though it has three distinct definitions in microwave applications as stated in [5]: power gain, available gain, and transducer power gain. Considering the transducer power gain for LNA design, that is by definition the ratio of the power delivered to the load to the power available from the source, its expression is given in [5] by:

$$G_T = \frac{|S_{21}|^2(1 - |\Gamma_S|^2)(1 - |\Gamma_L|^2)}{|1 - \Gamma_{in}\Gamma_S|^2|1 - S_{22}\Gamma_L|^2} [5] \quad (1)$$

Where:

- S_{11} : input reflection coefficient.
- S_{12} : reverse transmission gain.
- S_{21} : forward transmission gain.
- S_{22} : output reflection coefficient.
- Γ_S : Unconditioned source reflection coefficient.
- Γ_L : Unconditioned load reflection coefficient.
- Γ_{in} : Unconditioned input reflection coefficient.

And:

$$\Gamma_S = \frac{Z_S - Z_0}{Z_S + Z_0} [5] \quad (2)$$

$$\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0} [5] \quad (3)$$

$$\Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} [5] \quad (4)$$

Then the maximum unilateral transducer power gain could be derived from expression (1) under the conjugate matching condition at the input and output as mentioned in [6]:

$$\Gamma_L = S_{22}^* \text{ \& } \Gamma_S = S_{11}^* [5] \quad (5)$$

Consequently:

$$G_{TU,max} = \frac{1}{1 - |S_{11}|^2} |S_{21}|^2 \frac{1}{1 - |S_{22}|^2} [5] \quad (6)$$

B. Noise figure

By definition NF, noise figure is described as the amount of degradation of the SNR between the input and output of the component [5]. In low noise amplifier designs NF have to be minimized, though this minimization is restricted by multiple constraints and trade-offs such as the minimum noise figure could be achieved by a certain structure.

1) *Noise factor of a single stage LNA*: In a single stage low noise amplifier, the noise factor is given by expression (4) in [5]:

$$F = F_{min} + \frac{4R_N}{Z_0} \frac{|\Gamma_S - \Gamma_{opt}|^2}{(1 - |\Gamma_S|^2)(1 + |\Gamma_{opt}|^2)} \quad [5] \quad (7)$$

Where:

- F_{min} : minimum noise factor, achieved if $\Gamma_S = \Gamma_{opt}$.
- R_N : Equivalent noise resistance of the transistor, given by the constructor.
- Z_0 : Reference impedance.
- Γ_{opt} : the optimum input reflection coefficient, given by the constructor of the transistor.

2) *Noise factor of arbitrary LNA stage*: In case of several microwave stages, the overall noise figure is calculated using the following expression [5]:

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \dots \quad [5] \quad (8)$$

Where:

- F_n : the noise factor of the n^{th} stage.
- G_n : the gain of the n^{th} stage.

It must also be stated that:

$$NF = 10 \log_{10}(F) \quad [5] \quad (9)$$

That makes the noise factor a linear quantity, and the noise figure a logarithmic one.

C. Stability

Oscillations are a great threat to electronic devices as they serve as a source of parasites, these later occur when $|\Gamma_{in}| > 1$ or $|\Gamma_{out}| > 1$, therefore stability of the amplifier is achieved when $|\Gamma_{in}| < 1$ and $|\Gamma_{out}| < 1$, as stated in [5] two types of stability exist:

- **Unconditional stability**: that is if $|\Gamma_{in}| < 1$ and $|\Gamma_{out}| < 1$ for all passive load and source impedances.
- **Conditional stability**: That is if the condition $|\Gamma_{in}| < 1$ and $|\Gamma_{out}| < 1$ is verified only for a certain range of source and load impedances.

1) *Unconditional stability tests*: Before proceeding with stability circles to check for conditional stability, Rollet's conditions could be used to check for unconditional stability:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{|S_{12}S_{21}|} > 1 \quad [5] \quad (10)$$

$$\Delta = |S_{11}S_{22} - S_{21}S_{12}| < 1 \quad [5] \quad (11)$$

However recently a new criterion has been developed to check unconditional stability [5]:

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta S_{11}^*| + |S_{12}S_{21}|} \quad [5] \quad (12)$$

if $\mu > 1$ then the device is unconditionally stable.

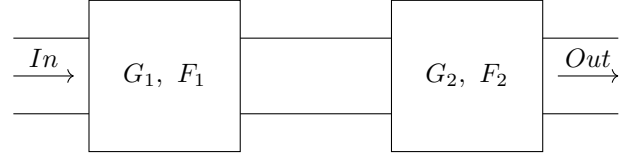


Fig. 1: The proposed topology

III. LNA DESIGN

A. Topology

The proposed topology of the LNA shown in figure:1, is a two stage topology that is formed by cascading two low noise amplifiers in order to maintain a low NF level and to reach a high power gain, the first goal could be explained using equation (8):

$$F_T = F_1 + \frac{F_2 - 1}{G_1} \quad (13)$$

Where: F_T is the total noise factor of the LNA, F_1 is the noise factor of the first stage, and F_2 is the noise factor of the second stage. Considering the fact that $G_1 \gg F_2 - 1$, the second term of F_T will tend to null, hence the total noise factor is only based on the noise factor of the first stage under the fact stated formally.

Using the signal flow graph representation of the network showed in 1, the total gain is easily obtained by applying the series decomposition rule:

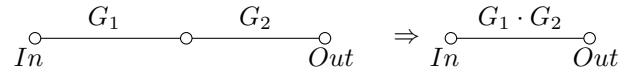


Fig. 2: Signal flow graph of the proposed topology

As it is shown in figure:2, the overall gain of the amplifier is equal to the multiplication of the linear gains of both stages, and the overall noise figure is given by equation (13).

B. Pre-amplifier stage design

1) *Transistor choice*: As the pre-amplifier stage imposes its noise figure upon the whole network, the selected transistor must possess a very low noise figure, from another side of view the gain of this stage is important also, as the noise factor of the second stage is suppressed by dividing on the pre-amplifier gain, hence the chosen transistor must have a relatively low NF and a high gain.

To preserve the criterions mentioned above the Infineon_BFP640 is chosen to design this LNA stage, this transistor is an high linearity radio frequency NPN bipolar junction transistor, its intrinsic composition is based on SiGe material, it could achieve 0.65dB noise figure and 24dB gain at 1.9GHz frequency [7].

2) *DC bias network*: The DC bias network represented in figure:3 will work as the activator of the transistor, it contains a resistive bridge R_2 and R_3 that polarizes the NP junction of the transistor beyond the threshold voltage V_{BE} so current could start flowing from the collector to the emitter, R_1 will provide enough voltage drop to each the intended voltage at the collector, the biasing is designed to obtain $I_c = 15mA$ and $V_{CE} = 2V$.

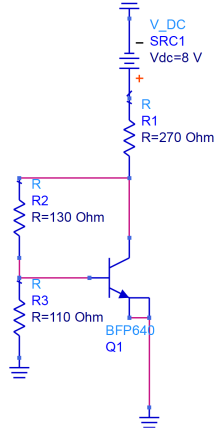


Fig. 3: DC bias network of the pre-amplifier

3) *Narrow band pre-amplifier*: After biasing the transistor correctly, the next step is to design input and output matching networks as shown in figure:4, for a first attempt this is going to be done on one frequency that is $5GHz$ i.e: *narrow band matching*, using the smith chart utility from keysight ADS simulation software, then broad band matching will be reached via tuning by means of the tuning tool in ADS. The stability check is going to take place in ADS by means of the criterion μ in equation (12), The [S] matrix is measured in ADS via the S_parameter simulator then Γ_{in} is calculated using equation (4), the output reflection coefficient is also obtained by means of the following equation:

$$\Gamma_{in} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \quad (14)$$

The source and load reflection coefficients are calculated by means of equations (2) and (3) respectively. The RF chokes L_{26} , L_{27} , and L_{28} are used to block RF energy from leaking to DC devices, while *DC_Block1* and *DC_Block2* are equivalent to high value capacitors used to block DC energy from flowing through the ports *TermG1* and *TermG2*.

The matching networks are open stub impedance matching networks, the dimensions of the stub and the transmission line are obtained from the smith chart tool that is used to realize conjugate reflection coefficient matching at the input and output, this is done to achieve the highest gain at $5GHz$, to achieve the lowest noise figure at the same frequency the input have to be matched to an optimum reflection coefficient as mentioned in equation (7), as Γ_{opt} is not given in [7], the dimensions of the input matching network have to be tuned to reach NF_{min} while maintaining the maximum gain.

Figure:5 shows the stability factor of the pre-amplifier stage, it is obvious that the circuit is stable at the intended frequency as $\mu > 1$.

From figure:6 it is remarkable that reflection coefficients have low values at $5GHz$, which is desired in microwave devices as they represent the amount of reflected power from the system to its injecting port, both S_{11} and S_{22} are below $-10dB$ which means that only 10% of the power is reflected at both ports.

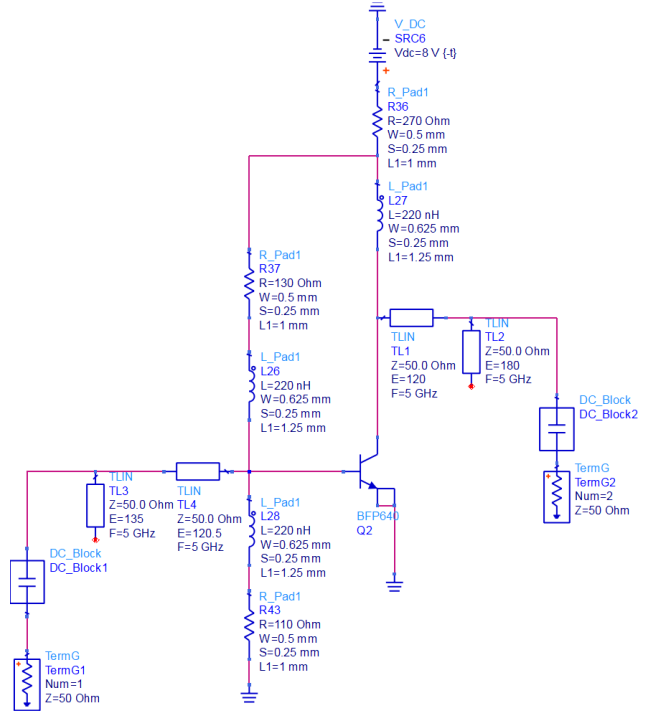


Fig. 4: Narrow band pre-amplifier schematic

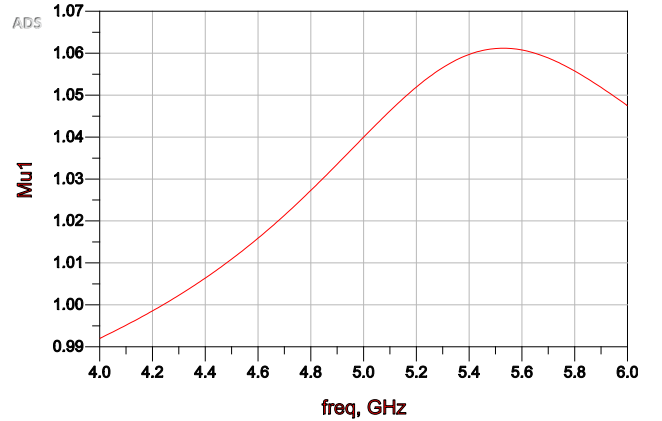


Fig. 5: narrow band pre-amplifier stability parameter μ

Figure:7 and figure:8 show that the pre-amplifier achieve the lowest noise figure at $5GHz$ which is the matching goal, the gain is also at almost its highest value, however the mismatch used to achieve NF_{min} at the input port produces a slight frequency shift on the gain curve, in other words it is often said that in a low noise amplifier the matching networks are used to achieve the lowest noise figure with the highest possible gain, that is reached in this narrow band pre-amplifier case.

4) *Broadband pre-amplifier*: The challenge now is to widen the bandwidth of the narrow band pre-amplifier in section III.B.3, for that reason the proposed matching networks used in that design represent an obstacle as they behave unexpectedly as shown in figure:9 and figure:10 at

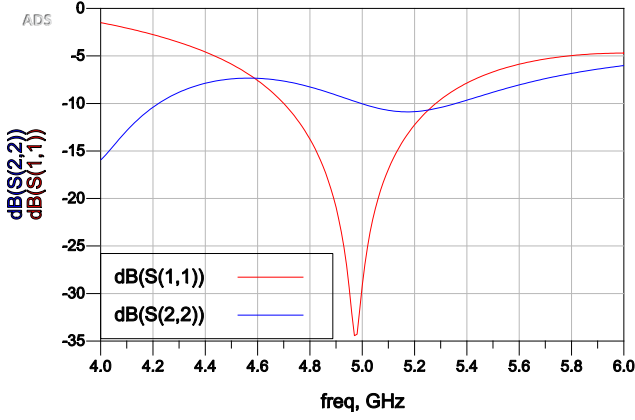


Fig. 6: narrow band pre-amplifier reflection coefficients

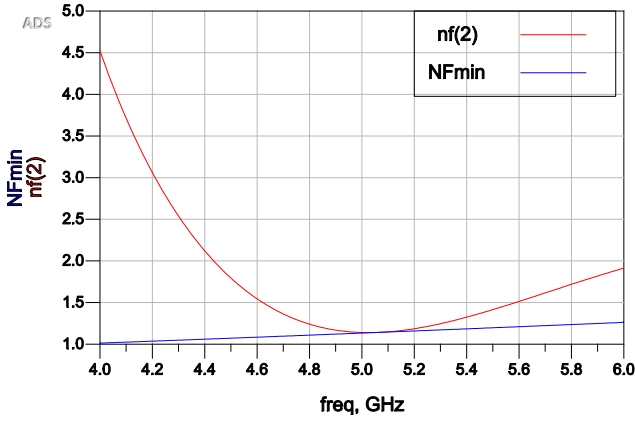


Fig. 7: narrow band pre-amplifier noise figure

the frequency band from 2 to 4.5GHz, this behavior is due to the S parameters susceptible to frequency variations as these matching networks are constructed from microstrip transmission lines.

Another topology is to be adopted to meet the wide band matching criterion that is to use a parallel LC network as shown in the input and output matching networks in figure:16, the values of the inductors and capacitors used in these matching networks are achieved via the tuning tool in ADS simulation software.

A one might propose to widen the bandwidth upwards to avoid the anomalies of the gain and the noise figure,

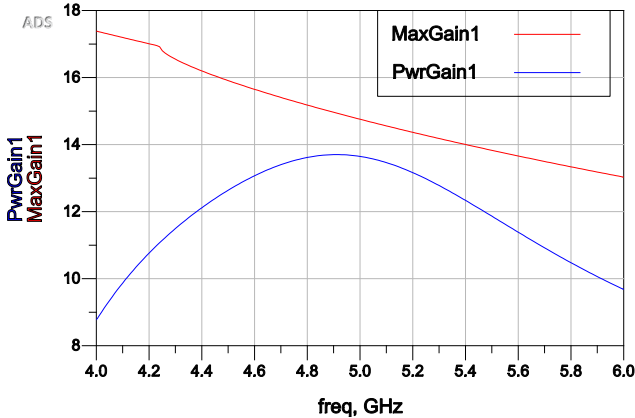


Fig. 8: narrow band pre-amplifier gain

that is not possible as the chosen transistors possess upper cutoff frequencies.

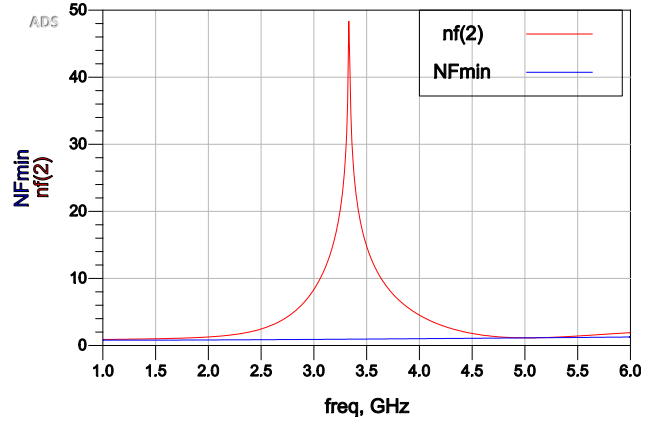


Fig. 9: narrow band pre-amplifier gain

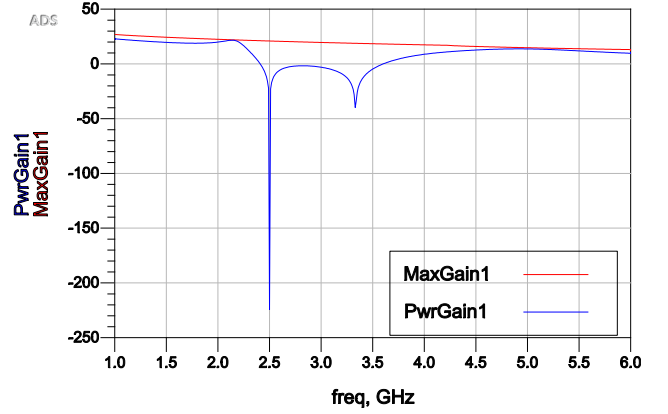


Fig. 10: narrow band pre-amplifier gain

It is necessary to clarify that all components included in the design shown in figure:16 are microstrip transmission lines used for the sake of interconnection to increase the level of convergence to real results, that includes: MLIN, MCROSO, Tee, MCURVE, and MTAPER, the component VIAGND is used to simulate the effect of microstrip via ground. The width of these lines is 2.5mm and their length varies upon the need.

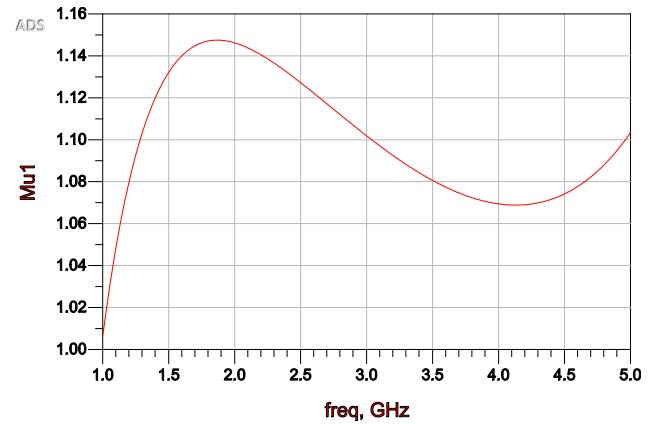
Fig. 11: Broad band pre-amplifier μ parameter.

Figure:11 shows that the pre-amplifier is unconditionally stable over a wide range of frequencies starting from

1 to 6GHz, this was achieved by adding a 10Ω resistor R_{44} at the input of the amplifier, however widening the stability bandwidth of the amplifier using this approach might affect the S_{11} parameter by mismatching the source 50Ω impedance that is why R_{44} is fixed at 10Ω .

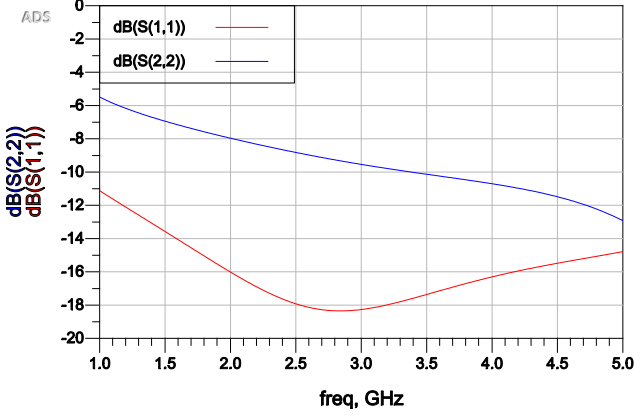


Fig. 12: Broad band pre-amplifier reflection coefficients.

Figure:12 shows that the input reflection coefficient is well beneath $-10dB$, however the output reflection coefficient is higher than $-10dB$, which is a disadvantage for such a device, however this is tolerable as an amplifier is not a reciprocal device that means that RF power will be injected always from port one to port two, as the parameter S_{22} concerns the amount of power reflected at port number 2 when the total power is injected from port 2 into the microwave system. This might not affect the LNA as a single device, however it will affect the impedance matching over a microwave network as port 2 impedance is almost mismatched.

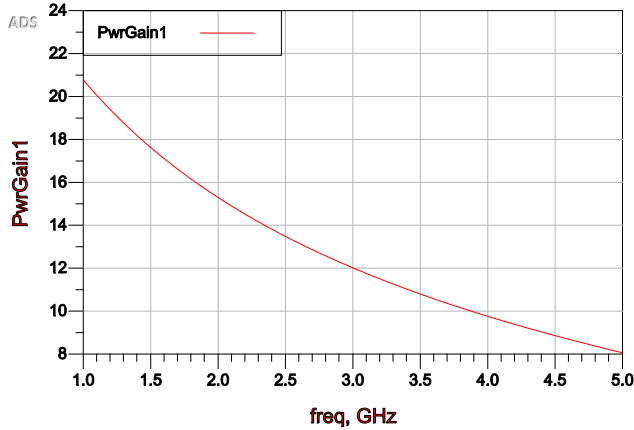


Fig. 13: Broad band pre-amplifier gain.

As depicted in figure:13 the gain of the pre-amplifier is above $8dB$ over the whole frequency band, however its decreasing aspect may affect the harmonic components as stated in [4], the main cause of this gain drop back to the S_{21} parameter decreasing shape of the BFP640 transistor [7].

The main parameter in a pre-amplifier is the noise figure, as represented in figure:14, NF of this device is excellent as it remains under $3dB$ over the whole frequency band.

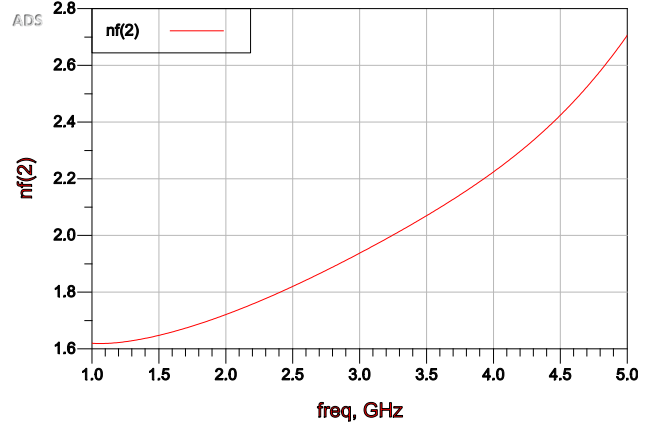
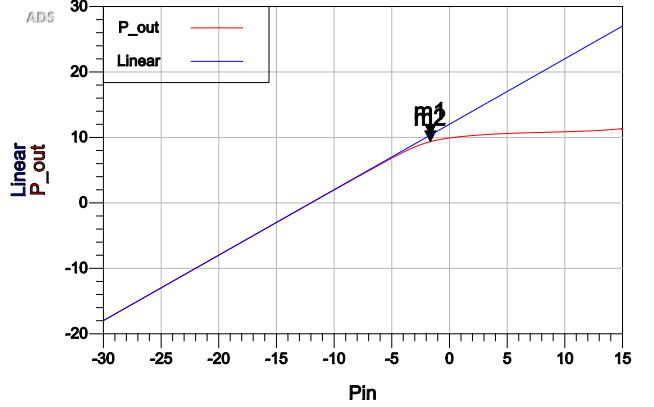


Fig. 14: Broad band pre-amplifier noise figure.



Pin	Pout	compression
-1.660	9.355	1.000

```

Eqn P_out=dBm(HB1.HB.Vout[:,1])
Eqn compression=m1-m2
Eqn Gain = dBm(HB1.HB.Vout[1])-Pin
Eqn Linear = Gain[0]+Pin
Eqn Pout=m2

```

m2
Pin=-1.660
P_out=9.355

m1
Pin=-1.660
Linear=10.355

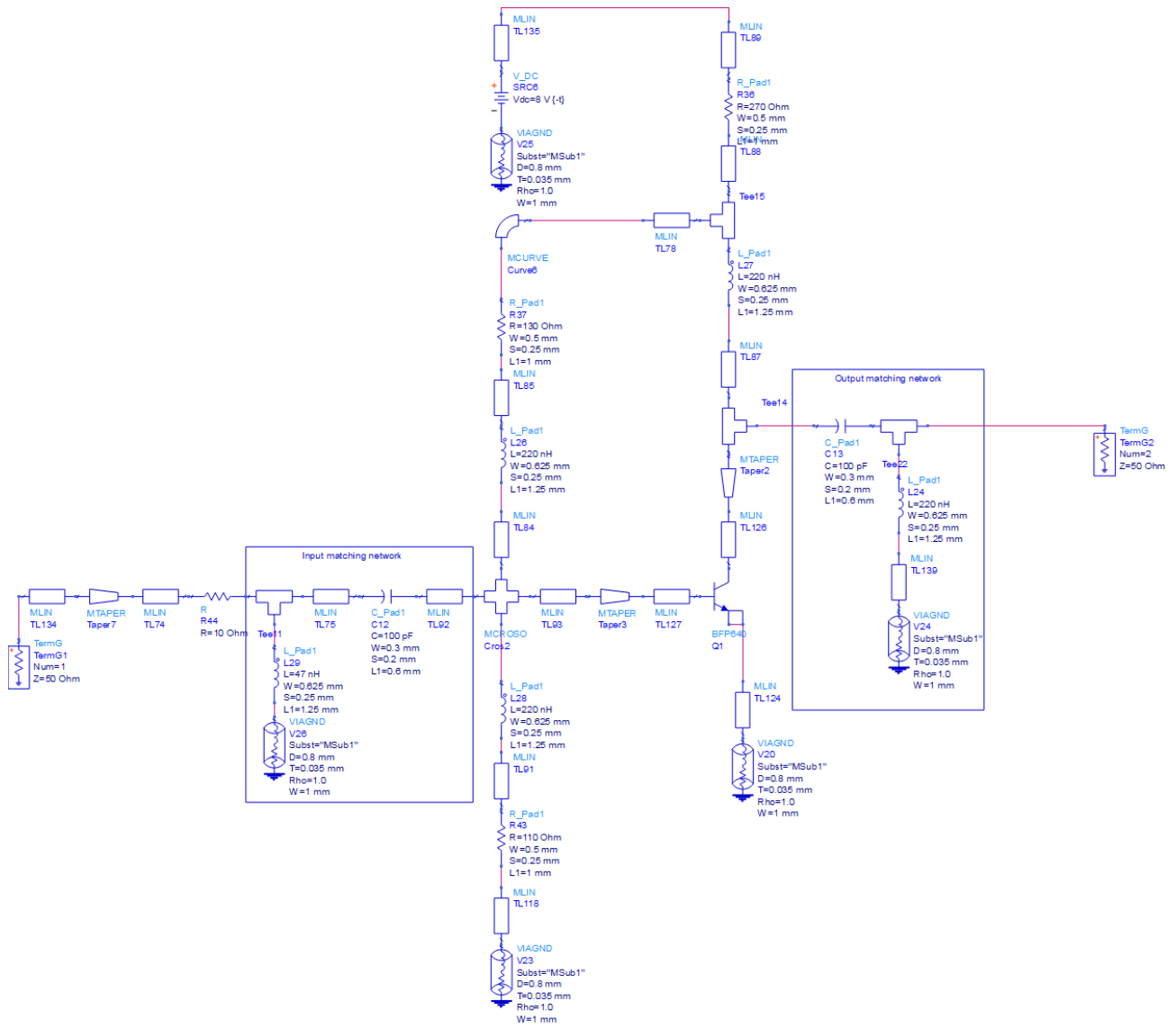
Fig. 15: Broad band pre-amplifier 1dB gain compression point..

Figure:15, shows the 1dB gain compression point, this point is achieved at an input power level $-11.070dB$ at $1GHz$.

The input and output third order intercept points are $12.62dB$ and $24.62dB$ respectively as illustrated in figure:17, both points “ADS_OIP3” and “ADS_IIP3” are calculated using measurements of harmonic balance simulation, however “OIP3” is calculated graphically for the sake of comparison using the equation $0.5 \cdot (3 \cdot m1 - m2)$ given in [8].

C. High gain stage design

1) *Transistor choice:* As noise figure here is of a second order importance, the high gain amplifier is built over the BFP420 [9], this transistor is a surface mount wideband silicon RF transistor, its characteristics are: $NF_{min} = 1.1dB$, $G = 21dB$ given at $1.8GHz$ frequency, as its decreasing gain characteristic with respect to fre-



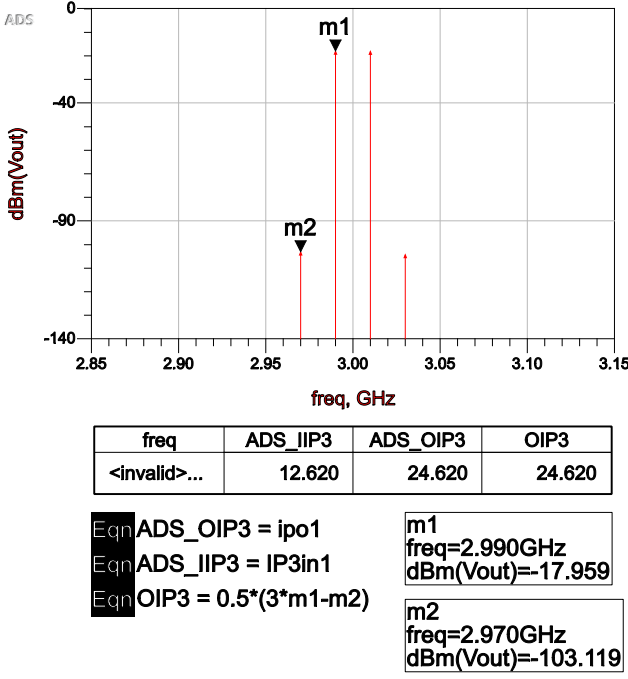


Fig. 17: Broad band pre-amplifier third order intercept point.

quency [9] that equals to 11dB at 5GHz it is suitable to increase the gain of the pre-amplifier over 10dB using the cascaded topology explained in III.A, another advantage is that its noise figure is below 3dB over the intended frequency band which makes it easy to be suppressed using the gain of the pre-amplifier. The design steps of this stage nearly the same as the formers, the main distinction lays is the broadband design in the next section.

2) *Broadband high gain amplifier*: The design of the high gain amplifier process is similar to the design of the pre-amplifier, the main distinction is that the high gain amplifier design goal is to reach the maximum achievable gain over the whole operating frequency band, noise figure is important here too, however it is not important to reach the minimum noise figure, the schematic of the high gain amplifier is illustrated in figure:24, the gain is achieved using the input and output matching networks, the R_{42} resistor at the output is used to reduce the mismatch level that is to decrease the parameter S_{22} .

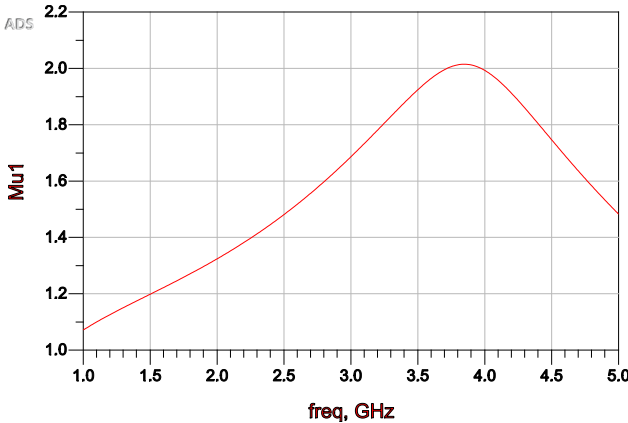


Fig. 18: Broad band high gain amplifier μ parameter.

The width of all microstrip interconnection transmission lines is 2mm that is tuned to never disturb the overall behavior of the circuit, however their length varies as necessary.

Figure:18 depicts the μ parameter of the high gain amplifier, as it is shown the curve is all above 1 over all the frequency band, as a result unconditional stability is achieved.

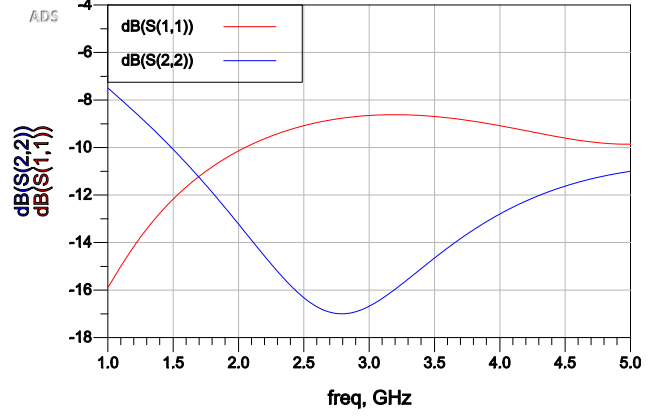


Fig. 19: Broad band high gain amplifier reflection coefficients.

Figure:19 shows the S_{11} and S_{22} parameters of the high gain amplifier.



Fig. 20: Broad band high gain amplifier gain.

The power gain of the amplifier is shown in figure:20, the gain drops from 18 to 4dB across the whole band that describes its poor gain linearity, however it is suitable to be used as a high gain block as the sum of both gain of the pre-amplifier and the high gain amplifier is about 12dB which satisfies the criterion stated in the specifications table:I.

Noise figure of this stage is illustrated in figure:21.

The 1dB compression point illustrated in figure:22 is obtained at 3GHz, the input power achieved at this point is -7.95dB, this point may vary along frequency variations which makes the amplifier more or less linear with respect to the input signal frequency. The input and output third order intercept points are 10.228dB and 22.228dB at 3GHz, both points are obtained via the measurement tool of the harmonic balance simulator in ADS, however OIP3 is obtained using the equation in [8].

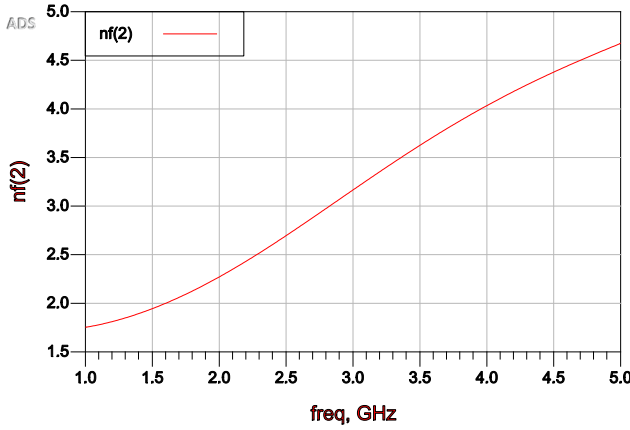


Fig. 21: Broad band high gain amplifier noise figure.

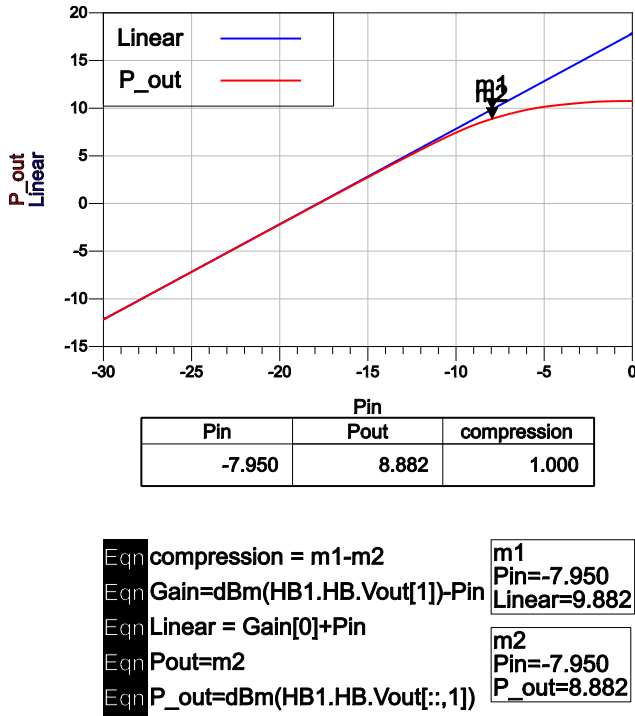
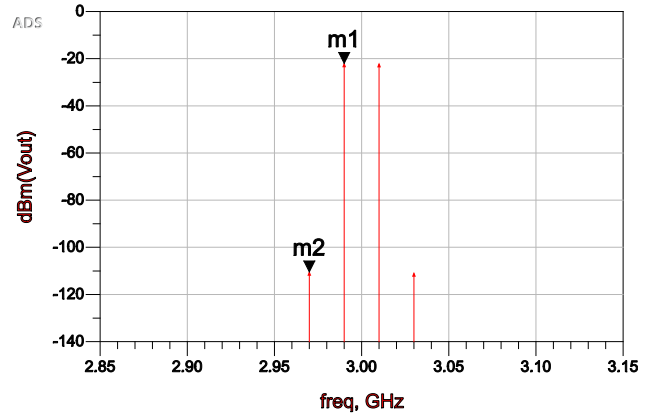


Fig. 22: Broad band high gain amplifier 1dB gain compression point.

D. Two stage LNA design

The proposed two stage amplifier is shown in figure: 30, the schematic has been slightly modified to widen the bandwidth toward $0.5GHz$ instead of starting at $1GHz$, that leads to guarantee unconditional stability over all the frequency band $[0.5 - 5]GHz$, the reflection coefficient S_{11} must also be below $-10dB$, and the power gain must be above $10dB$, the modifications done to achieve these specifications where: removing the resistor R_{44} at the input of the first stage to avoid high noise figure, each one of the emitters of both transistors is linked to the ground on its own, this helps reducing reflections also, the capacitor C_{16} is added as a linking capacitor, this helps isolating the stages, consequently achieving the intended goals.

The simulation strategy adopted through this section is different from previous sections, as the thoughts are to increase the reliability of simulation to decrease the gap between real and simulated results, consequently the co-



freq	ADS_IIP3	ADS_OIP3	OIP3
<invalid>...	10.228	22.228	22.228

Eqn ADS_IIP3=IP3in1	m1
Eqn ADS_OIP3=ipo1	freq=2.990GHz
Eqn OIP3=0.5*(3*m1-m2)	dBm(Vout)=-21.983
	m2
	freq=2.970GHz
	dBm(Vout)=-110.404

Fig. 23: Broad band high gain amplifier third order intercept point.

simulation method is adopted in ADS. The co-simulation is a simulation method that combines EM simulation of a layout with schematic simulation of components that could not be EM simulated.

The followed process is mentioned in the bullets below:

- Connect the pre-amplifier and the high gain amplifier to form the complete two stage low noise amplifier schematic.
- Check for components modifications using schematic simulation, that is to check weather they are in the correct ranges for the new schematic.
- Generate a circuit layout using ADS layout generator.
- Modify the lengths of transmission lines and design footprints for electronic components, a second reason is to provide the ability to place schematic simulated components.
- Add ports at all positions from input and output of the LNA to component pins and DC supply voltage, that is to avoid open circuits as footprints are constructed from gaps mostly.
- Simulate the structure using EM simulator in ADS layout, that would generate the EM model view of the structure which contains the S parameters of the structure.
- Generate a symbol from the simulated layout.
- Include the symbol to a new schematic and place all schematic simulated components at their positions.
- Perform the co-simulation and evaluate results.

E. Simulation results

Figure:25 depicts the μ parameter of the two stage low noise amplifier shown in figure:30, as the curve is all above 1 unconditional stability is achieved over the frequency band $[0.5 - 5]GHz$. Input and output reflection coefficients

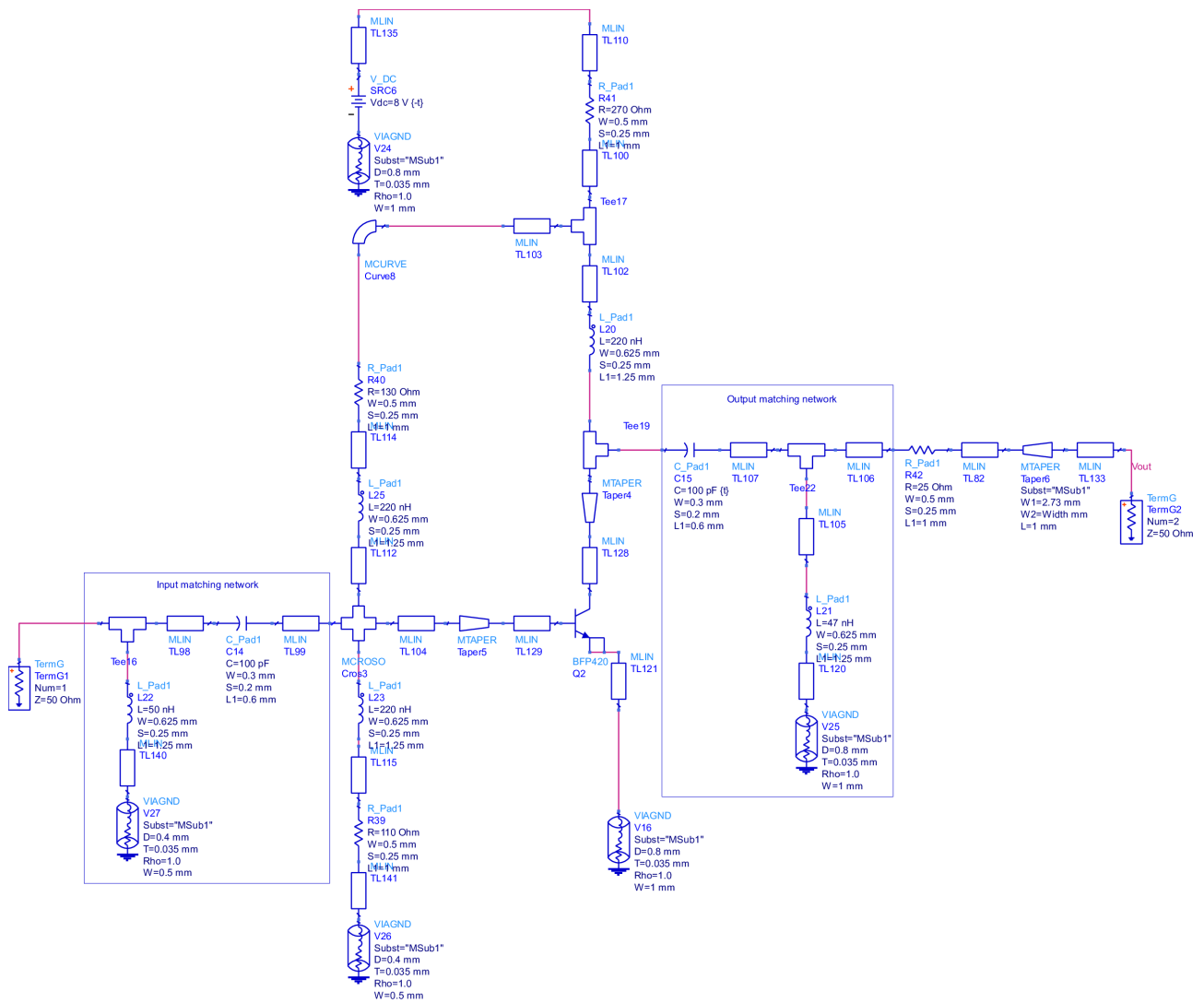


Fig. 24: Broad band high gain amplifier schematic

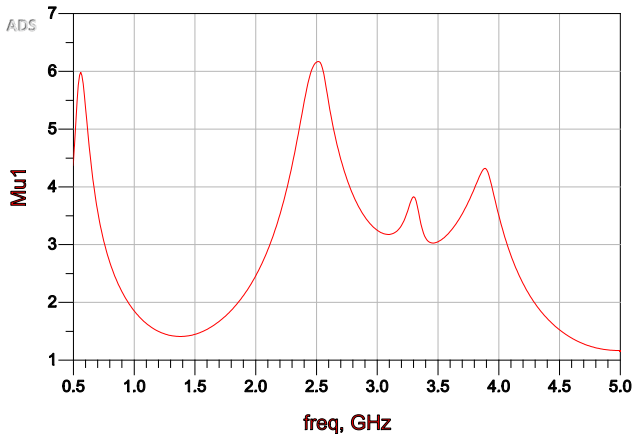


Fig. 25: Two stage low noise amplifier μ parameter.

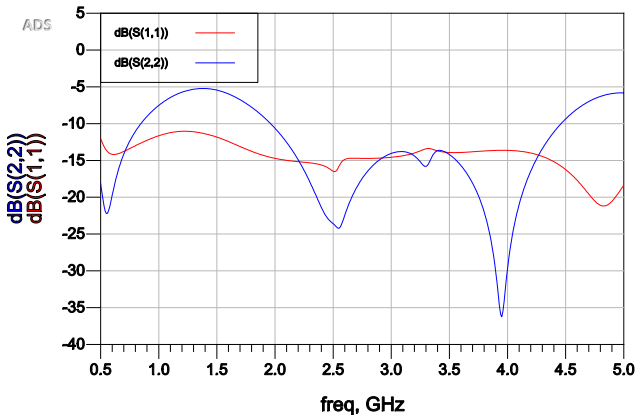


Fig. 26: Two stage low noise amplifier reflection coefficients.

are illustrated in figure:26, the $S_{11} < -10dB$ condition is achieved as its curve is below that level over the frequency band $[0.5 - 5]GHz$, port 2 suffers from some reflections as S_{22} gets high at the beginning and ending of the band, however as an LNA is a non-reciprocal device reflections at port 2 are not important as power is injected at port 1 forever.

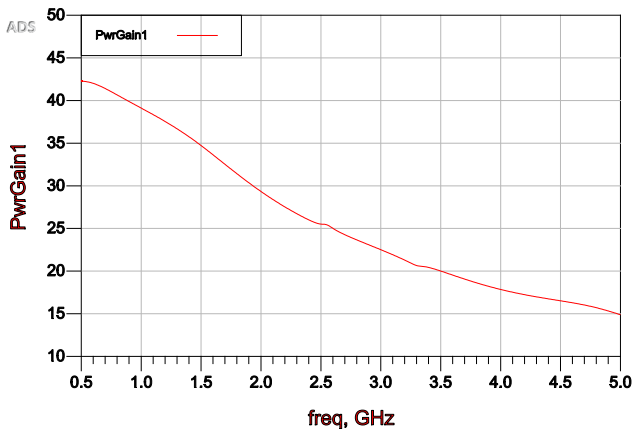


Fig. 27: Two stage low noise amplifier gain.

Figure:27 illustrates the power gain of the two stage low noise amplifier, the decreasing aspect of the curve returns to the decreasing curve of the transistors themselves as shown in their datasheet [9] [7], despite that the

gain constraint $G > 10dB$ has been achieved as its curve is above $14dB$ across the intended frequency band.

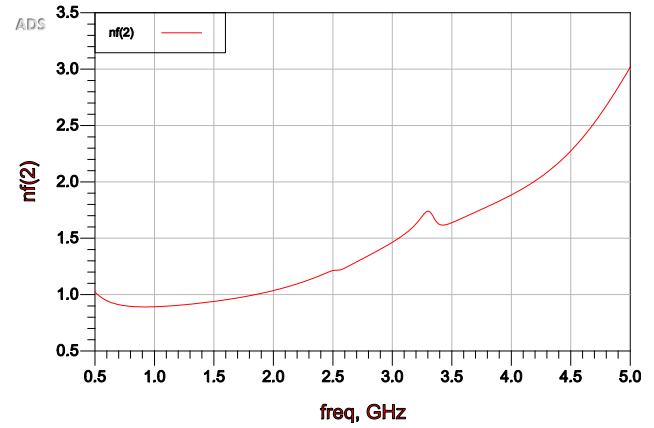
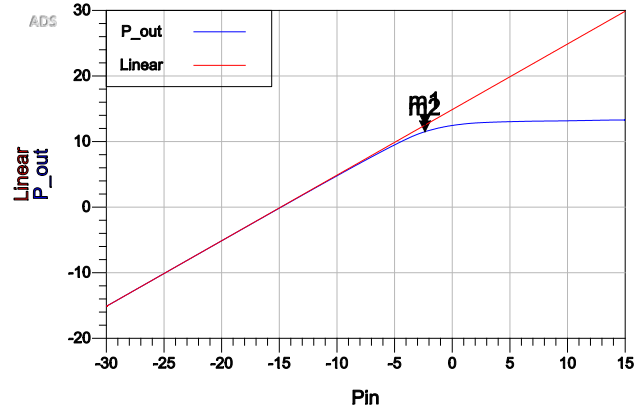


Fig. 28: Two stage low noise amplifier gain.

The noise figure of the two stage LNA is shown in figure:28, as the curve is below the $3dB$ level, the noise figure criterion is achieved.



Pin	Pout	compression
-2.370	11.505	1.002

```

Eqn Gain1=dBm(HB1.HB.Vout[1])-Pin
Eqn P_out = dBm(HB1.HB.Vout[:,1])
Eqn compression = m1-m2
Eqn Linear = Gain1[0]+Pin
Eqn Pout=m2

```

m1
Pin=-2.370
Linear=12.507

m2
Pin=-2.370
P_out=11.505

Fig. 29: Two stage low noise amplifier gain.

Figure:29 shows the $1dB$ compression point, for this LNA this point is achieved at $-2.370dBm$ input power at $5GHz$, consequently all signals below this power level are sentenced to experience a linear behavior of the amplifier, above this power level all signals are compressed as depicted in figure:29 P_{out} plot.

Figure:31 shows the input and output third order intercept points, their levels are: $7.764dBm$ and $22.094dBm$ respectively, for a low noise amplifier the $IIP3$ point is the most important, though it guarantees the linear behavior of the amplifier below its value as the contribution of third order harmonics is minimized as shown in figure:31, above the $IIP3$ point third order harmonics gain enough strength

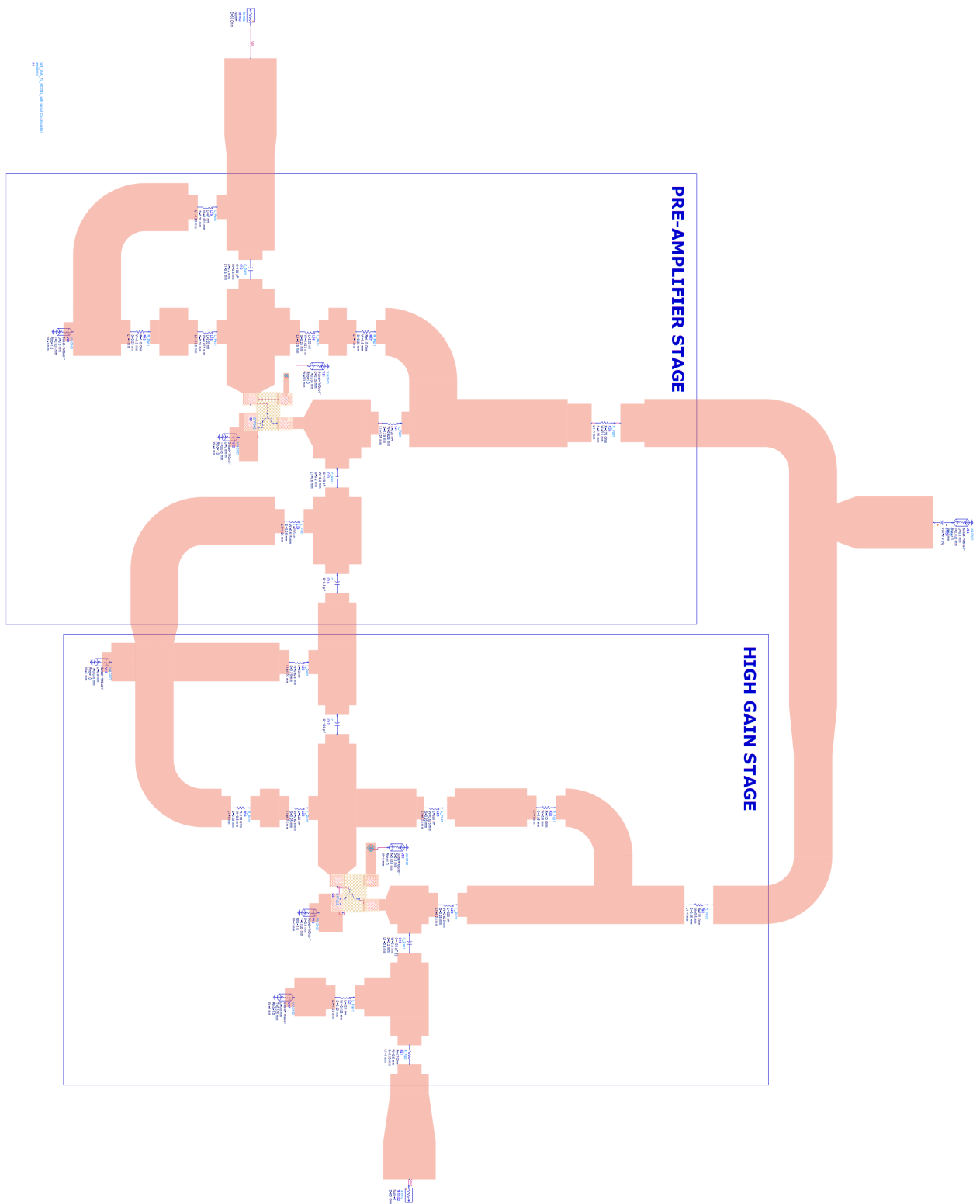


Fig. 30: Broad band high gain amplifier schematic

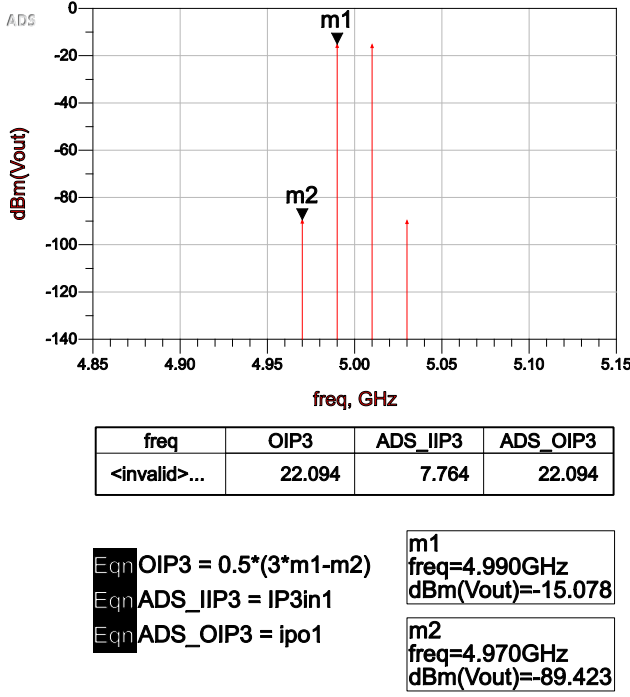


Fig. 31: Two stage low noise amplifier third order intercept point.

to contribute to the output signal, consequently the input and output signals have no longer the same spectrum as intermodulation terms have contributed significantly to the input signal.

IV. CONCLUSION

Upon considering all the facts, this article contained a proposition of a microwave device which is a wideband low noise amplifier, the document contained the design and simulation results of each step of the circuit supported with interpretations and discussions. The main challenge was to guarantee the specifications of the LNA across a wideband, however this challenge was accomplished correctly.

Consequently the LNA had a wide operating band that is $[0.5 - 5]GHz$, an acceptable gain over $14dB$, a low noise figure that is below $3dB$, the S_{11} parameter was below $10dB$ which refers to a fine matching at the input, these parameters are preserved across the whole frequency band stated before.

The $1dB$ compression point was at $-2.37dBm$ input power, that is signals with power higher than this level are compressed to the output power level at the $1dB$ gain compression point due to the non linear behavior of the amplifier after that point, the third order input intercept point $IIP3$ is $7.764dBm$, that is the power difference between the fundamental frequency and the third order harmonics of equation $f_c \pm 2\Delta f$ where Δf is $100MHz$, and f_c is the fundamental frequency, the third order output intercept point $OIP3$ is a measure of distortion and linearity of the LNA, a higher $OIP3$ and $IIP3$ means a higher difference between the fundamental and the third order harmonic, which consequently yields a good linearity and less distortion.

Finally our future aims are to produce these simulation results in reality by means of measurements to add more support to the proposed design.

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